CLAIMS

1. A method comprising:

impinging laser energy on a substrate; and

effecting laser-induced cleaving of the substrate.

2. A method as claimed in claim 1, comprising:

effecting a predetermined material within the substrate to form a predetermined cleave layer;

impinging predetermined laser energy on the material to effect the laser-induced cleaving of the substrate, within the cleave layer.

3. A method as claimed in claim 2, wherein the substrate comprises silicon (Si), the predetermined material comprises germanium (Ge), and the laser energy is tuned to be greater than a band gap of SiGe but smaller than that of Si.

4. A method as claimed in claim 2, wherein the substrate comprises silicon (Si), the predetermined material comprises hydrogen (H), and the laser energy is infrared laser energy.

5. A method as claimed in claim 2, wherein the laser energy induces selective bond breaking at an interface of a host material of the substrate and the predetermined material, to effect the laser-induced cleaving of the substrate, substantially along the interface.

6. A method as claimed in claim 2, comprising at least one of:

stoichiometrically designing a composition of the material to substantially match a bond breaking energy involving the material, to the predetermined laser energy; and,

selecting the predetermined laser energy to substantially match a bond-breaking threshold energy of the material, based upon at least a stoichiometric composition of the material.

7. A method as claimed in claim 6, comprising predetermined balancing of a stoichimetric composition of the material verses a degree of the predetermined laser energy to effect a predetermined cleave yield.

8. A method as claimed in claim 2, comprising:

bonding the substrate to a receiving substrate prior to the laser-induced cleaving, wherein upon the laser-induced cleaving, a layer cleaved from the substrate remains bonded to the receiving substrate.

9. A method as claimed in claim 1, comprising:

using simultaneous application of a plurality of interfering laser beams to effect the predetermined laser energy to effect the laser-induced cleaving substantially along a laser-defined cleave plane.

10. A method as claimed in claim 9, comprising:

the plurality of interfering laser beams having at least one of specifically tuned energies, incidence angles and/or space profiles, to define a desired cleave plane.

11. A method as claimed in claim 9, comprising:

designing a profile of a laser energy interference pattern to define depth of a desired cleave plane.

12. A method as claimed in claim 9, comprising:

effecting a predetermined material within the substrate to form a predetermined cleave layer, within which the laser-induced cleaving is to be effected.

13. A method as claimed in claim 12, wherein the substrate comprises silicon (Si), the predetermined material comprises germanium (Ge), and the laser energy is tuned to be greater than a band gap of SiGe but smaller than that of Si.

14. A method as claimed in claim 12, wherein the substrate comprises silicon (Si), the predetermined material comprises hydrogen (H), and the laser energy is infrared laser energy.

15. A method as claimed in claim 12, wherein the laser energy induces selective bond breaking at an interface of a host material of the substrate and the predetermined material, to effect the laser-induced cleaving of the substrate, substantially along the interface.

16. A method as claimed in claim 12, comprising at least one of:

stoichiometrically designing a composition of the material to substantially match a bond breaking energy involving the material, to the predetermined laser energy; and,

selecting the predetermined laser energy to substantially match a bond-breaking threshold energy of the material, based upon at least a stoichiometric composition of the material.

17. A method as claimed in claim 16, comprising predetermined balancing of a stoichimetric composition of the material verses a degree of the predetermined laser energy to effect a predetermined cleave yield.

18. A method as claimed in claim 9, comprising:

bonding the substrate to a receiving substrate prior to the laser-induced cleaving, wherein upon the laser-induced cleaving, a layer cleaved from the substrate remains bonded to the receiving substrate.

19. A method as claimed in claim 1, comprising:

impinging the laser energy on at least one side edge of the substrate in a side-cut mode in effecting the laser-induced cleaving.

20. A method as claimed in claim 19, comprising:

effecting a predetermined material within the substrate to form a predetermined cleave layer;

impinging predetermined laser energy on the material to effect the laser-induced cleaving of the substrate, within the cleave layer.

21. A method as claimed in claim 20, wherein the substrate comprises silicon (Si), the predetermined material comprises germanium (Ge), and the laser energy is tuned to be greater than a band gap of SiGe but smaller than that of Si.

22. A method as claimed in claim 20, wherein the substrate comprises silicon (Si), the predetermined material comprises hydrogen (H), and the laser energy is infrared laser energy.

23. A method as claimed in claim 20, wherein the laser energy induces selective bond breaking at an interface of a host material of the substrate and the predetermined material, to effect the laser-induced cleaving of the substrate, substantially along the interface.

24. A method as claimed in claim 20, comprising at least one of:

stoichiometrically designing a composition of the material to substantially match a bond breaking energy involving the material, to the predetermined laser energy; and,

selecting the predetermined laser energy to substantially match a bond-breaking threshold energy of the material, based upon at least a stoichiometric composition of the material.

25. A method as claimed in claim 24, comprising predetermined balancing of a stoichimetric composition of the material verses a degree of the predetermined laser energy to effect a predetermined cleave yield.

26. A method as claimed in claim 19, comprising:

forming micro-voids in the substrate prior to impinging the laser energy on the at least one side edge of the substrate in the side-cut mode, and effecting the laser-induced cleaving along a cleave plane defined by ones of the micro-voids.

27. A method as claimed in claim 20, wherein the substrate comprises silicon (Si), wherein the micro-voids are formed by implantation of at least one of hydrogen (H), H2 and helium (He) into the substrate, and subsequent annealing of the substrate.

28. A method as claimed in claim 19, comprising:

bonding the substrate to a receiving substrate prior to the laser-induced cleaving, wherein upon the laser-induced cleaving, a layer cleaved from the substrate remains bonded to the receiving substrate.

29. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 1.

30. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 2.

31. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 3.

32. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 4.

33. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 5.

34. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 6.

35. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 7.

36. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 8.

37. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 9.

38. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 10.

39. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 11.

40. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 12.

41. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 13.

42. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 14.

43. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 15.

44. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 16.

45. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 17.

46. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 18.

47. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 19.

48. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 20.

49. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 21.

50. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 22.

51. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 23.

52. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 24.

53. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 25.

54. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 26.

55. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 27.

56. A system comprising:

at least one item selected from a list of: an electronic package, PCB, socket, bus portion, input device, output device, power supply arrangement and case; and

at least one silicon-on-insulator semiconductor device manufactured through use of at least the method of claim 28.